utrf.tennessee.edu
gsechris@tennessee.edu
(865) 974-1882
400 W. Summit Hill Drive
UT Tower 961A
Knoxville, TN 37902

Neuromorphic Computing & Memristive Technologies

About TENNLab

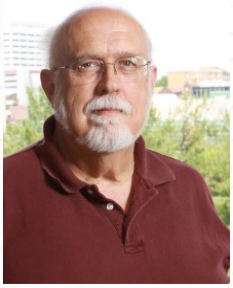
As Moore's law comes to an end, there is a growing need for alternative approaches to traditional computing architectures to continue increasing performance on chip. Machine learning is an integral component to post Moore's law innovation, and while deep learning models have proven useful in areas such as image classification and sentiment analysis, they still struggle with time-dependent, dynamic environments.

Brain inspired, spiking neural networks offer promises of low energy dissipation, co-location of memory and computation, inherent stochasticity, and dynamic architectures for machine learning applications. Leveraging these advantages, a group of researchers at The University of Tennessee have developed hardware and software to aid in the development of these revolutionary computing paradigms. The technologies presented in this brochure represent the years that these researchers have dedicated to revolutionizing neuromorphic computing technologies.

Click here to learn more about TENNLab.

Inventors

TENN LAB NEUROMORPHIC ARCHITECTURES. LEARNING. APPLICATIONS.



DR. DOUG BIRDWELL

DR. AHMEDULLAH AZIZ

DR. GARRETT ROSE

DR. KATIE SCHUMAN

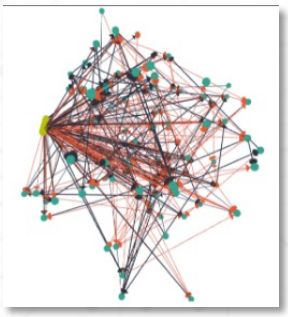
DR. JAMES PLANK

DR. MARK DEAN

Computing Models

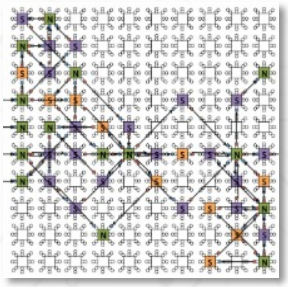
Inventions

The TENNLab has developed three novel frameworks for dynamic, spiking neural networks. The first framework, Neuroscience Inspired Dynamic Architecture (NIDA), represents neurons and synapses in 3-D space in a simulation framework and is trained using an evolutionary algorithm. Another framework, Dynamic Adaptive Neural Network Arrays (DANNA), is a 2-D model designed specifically for digital elements that are programmable as either neurons or synapses. The DANNA model was further developed into mrDANNA, leveraging memristors for energy-efficient, analog memory storage for synaptic weights. These technologies have been validated in simulation, FPGA implementation and integrated circuit layouts for real world applications, such as data classification, robot navigation, autonomous video game playing, pendulum balancing, handwritten digit classification, spoken language recognition, and anomaly detection in packet rates.



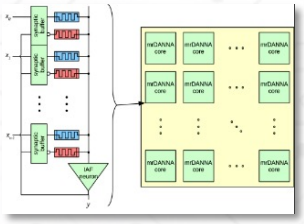
Neuroscience Inspired Dynamic Architecture (NIDA)

- Neurons and synapses laid out in 3D space
- Synaptic delays based on distance
- Implemented in software



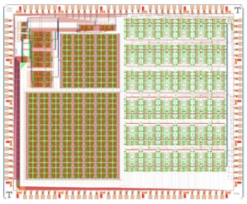
Dynamic Adaptive Neural Network Arrays (DANNA)

- 2-D Grid of Elements
- Elements can be either neurons or synapses
- FPGA implementation deployed
- VLSI implementation designed



Memristive Dynamic Adaptive Neural Network Arrays (mrDANNA)

- Leverages analog memristive hardware
- More flexible connectivity and delays



mrDANNA Integrated Circuit

Issued Patents

#1 US9753959

#2 US9798751

#3 US10019470

#4 US10055434

#5 US10095718

#6 US10248675

#7 US10929745

Memristive Technologies

Analog Memory Read Write Circuit Using Current-Controlled Elements

Dr. Garrett Rose has developed a novel method to read and write analog memory based on memristors using a specialized current control technique. The circuit uses six transistors for the read/write operation and one, two-terminal NVM element for the analog memory. It is highly tunable to many different resistance ranges, making it ideal for SNN circuits that need variable resistances for synaptic weights. The current-control mechanism refers to the control of a constant current which dictates how the NVM elements switch from a high resistance state to a low resistance state.

These analog memory cells may be used in a variety of applications, with one use case being to provide very dense storage of continuous synaptic weights in a brain-inspired computer system, such as in a machine learning accelerator or neuromorphic computing engine.

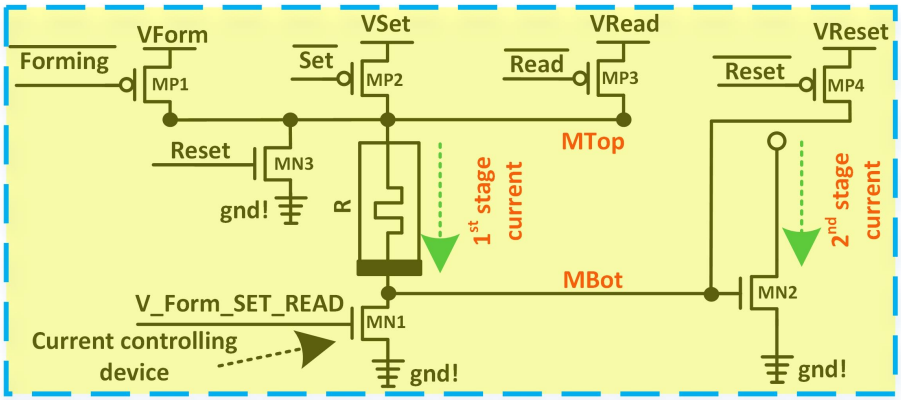


Illustration of the current-controlled memristive memory element for the Analog Memory Read Write Circuit.

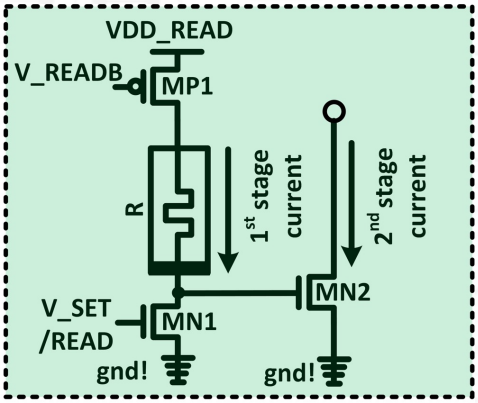


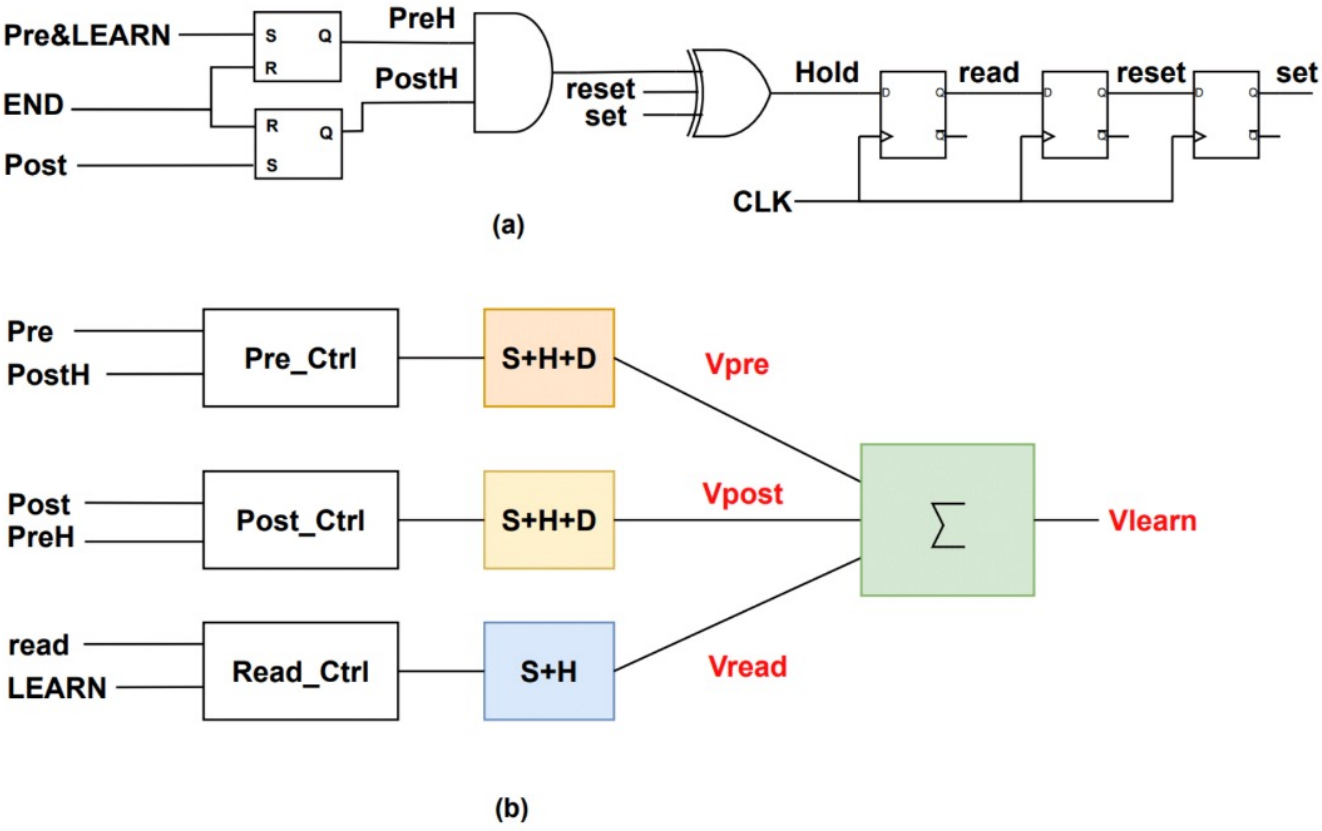
Illustration of the current-controlled memristive memory element for the Analog Memory Read Write Circuit.

This technology is patent pending.

Memristive Technologies

Spike Time Dependent Plasticity Implementation for Online Learning

Dr. Garrett Rose has developed a method of implementing Spike Time Dependent Plasticity (STDP) for online learning which is highly reliable and can be adapted to many different non-volatile analog memory devices. Using a current control mechanism to read and write from memristor based synapses, this circuit operates unsupervised while offering high reliability and component tunability.



Block Diagram of STDP Circuit (a) shows digital control circuit to update synaptic weight (b) shows the circuits used to generate the new voltage for controlling the applied current value.

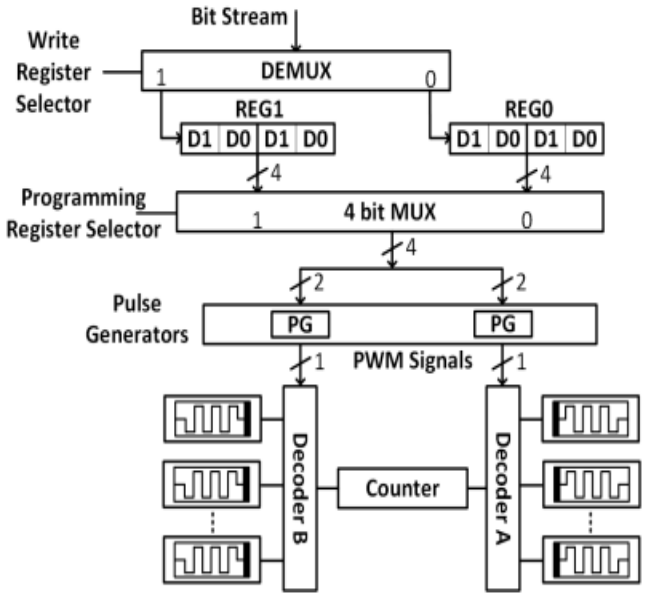
This technology is patent pending.

Non-Volatile Memory

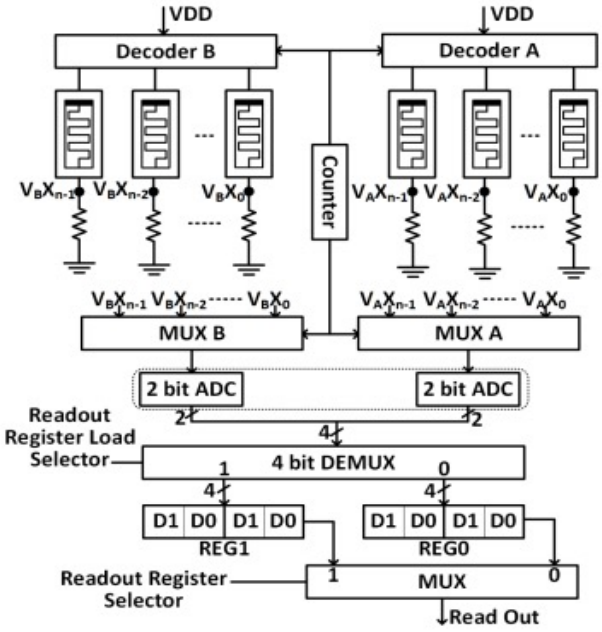
Scan Register Based Access Scheme for Multilevel Non-Volatile Memory

Dr. Garrett Rose has developed a system level scheme to configure or extract multi-bit information from Non-Volatile Memory (NVM) devices. The distributed NVM elements may be written using the proposed invention by scanning memory states sequentially into temporary scan registers and using these temporary values to write to NVM elements within a corresponding memory bank.

The scan registers can also be used to read out data bits from the non-volatile memory devices. To facilitate read and write operations, two scan registers are used interchangeably to separate and parallelize the programming/reading and shifting in/out of data bits. The proposed scheme can be scaled up to facilitate an arbitrarily high number of NVM devices with very limited increase of peripheral circuitry.



Block Diagram of Programming Scheme



Block Diagram of Reading Scheme

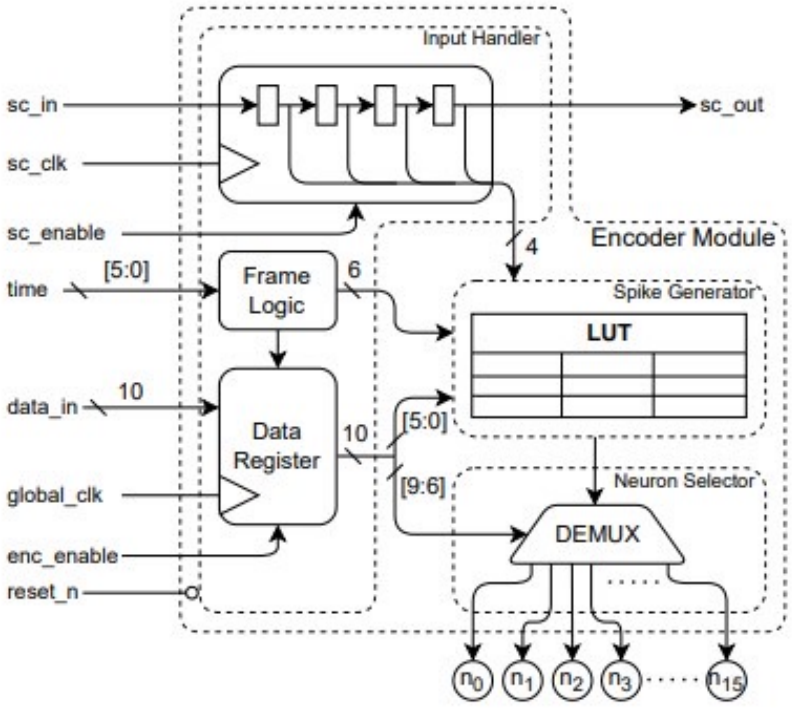
This technology is patent pending.

Spiking Neural Network Hardware

A Runtime-Reconfigurable Hardware Encoder for Spiking Neural Networks

Dr. Garrett Rose has developed a hardware implementation of a spike encoder which offers real-time encoding of sensor and real-world interface data into a spiking neural network (SNN) in three different encoding techniques. Encoding external data into spikes has remained largely a software endeavor for SNNs, but this delays the neuroprocessor by interrupting the neural network while a pre-processing CPU encodes the data and packetizes it. A hardware encoder can accelerate the spike encoding procedure by routing encoded spikes directly to the SNN and by avoiding pre-processing.

The hardware consists of an input handler which determines the encoding frame and handles the value to be translated into the spike train, a spike generator consisting of a look-up-table which generates the spike according to the chosen encoding method, and a neuron selector which routes the spike to the appropriate neuron or neuron cluster. Thanks to the reconfigurable nature of the encoder, multiple sensors could be connected to the encoder each



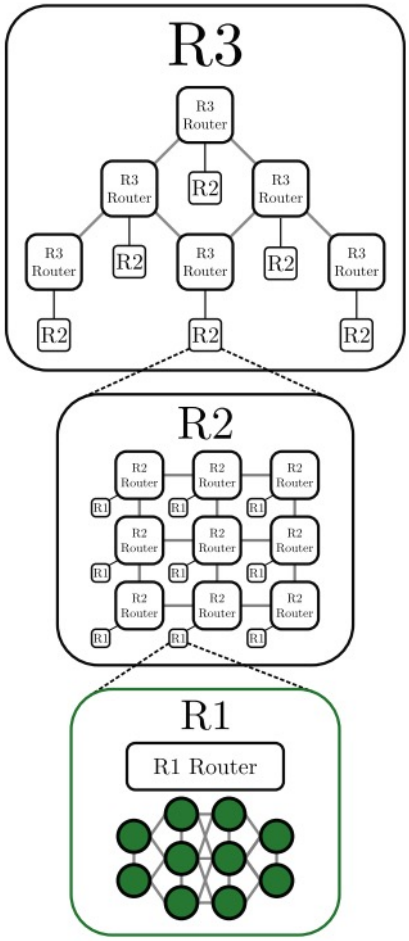
Block Diagram of the Hardware Encoder. After the encoding method is determined, information about time-step and the value to encode is used in a look-up-table to output and route a spike to a destination neuron.

This technology is patent pending.

Spiking Neural Network Communication Class Optimization

A Hierarchical Network-on-Chip Architecture for Globally Sparse, Locally Dense Communication Systems

Dr. Garrett Rose has developed a three-level network-on-chip architecture which prioritizes and optimizes different metrics at each level of the hierarchy. At level R1, a Clos network topology supports high data-integrity and power efficiency at the densest neuron level, with a switch to packetized AER communication occurring at the next two levels. At level R2, organization of neurons in a mesh architecture directs AER packets in such a way that favors bandwidth for route flexibility. Finally, at level R3, neural arrays are connected in a tree topology which favors low latency over comparatively longer distances.



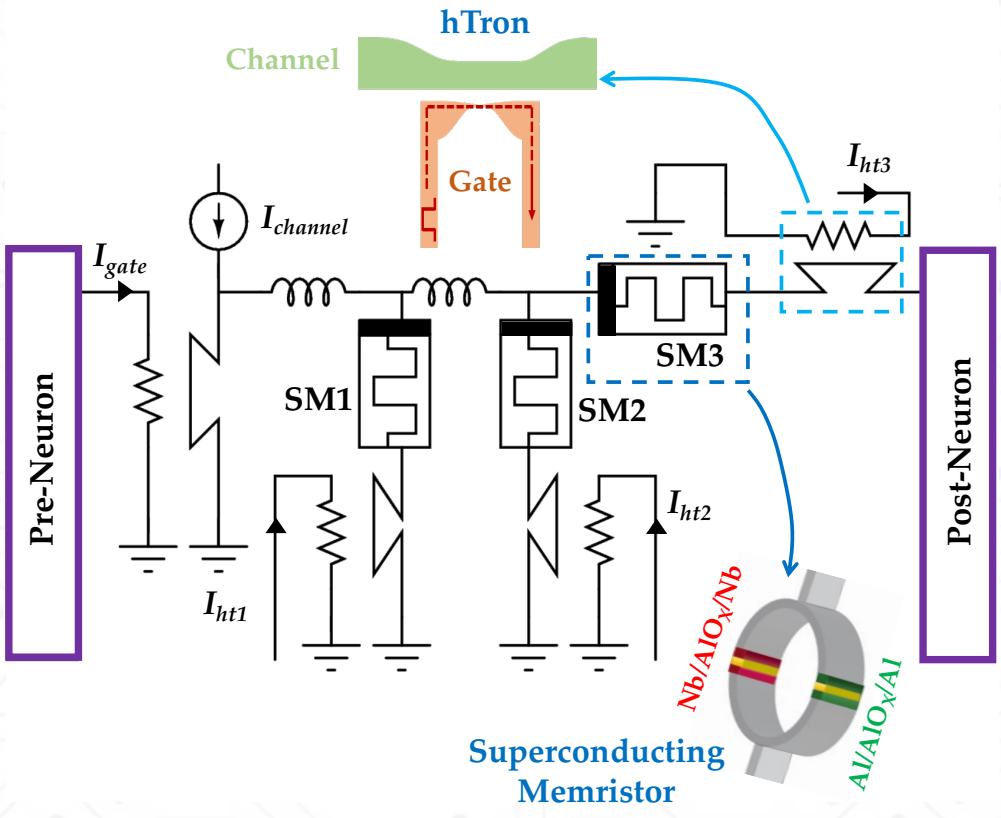
An illustration of the three-tiered hierarchical NoC structure showing the R1 Clos topology, R2 mesh topology, and R3 tree topology

This technology is patent pending.

Cryogenic Neuromorphic Hardware

A Cryogenic Artificial Synapse based on a Superconducting Memristor

Dr. Ahmedullah Aziz has developed an artificial synapse topology utilizing the coupled interactions between two unique superconducting devices – superconducting memristor (SM) and heater cryotron (hTron). The proposed synapse topology, combined with the SM-based neurons, can lead to a cryogenic neuromorphic system with lower energy consumption, better reconfigurability, and more effective synaptic weight programming than the existing cryogenic synapse structures. The proposed technology offers eight (8) different non-volatile levels of synaptic strength created from a combination of three (3) superconducting memristors with an estimated programming power of 8.5 pW. The non-volatile synapse-structure offers ultra-low energy consumption on the order of 10 aJ per spiking event.



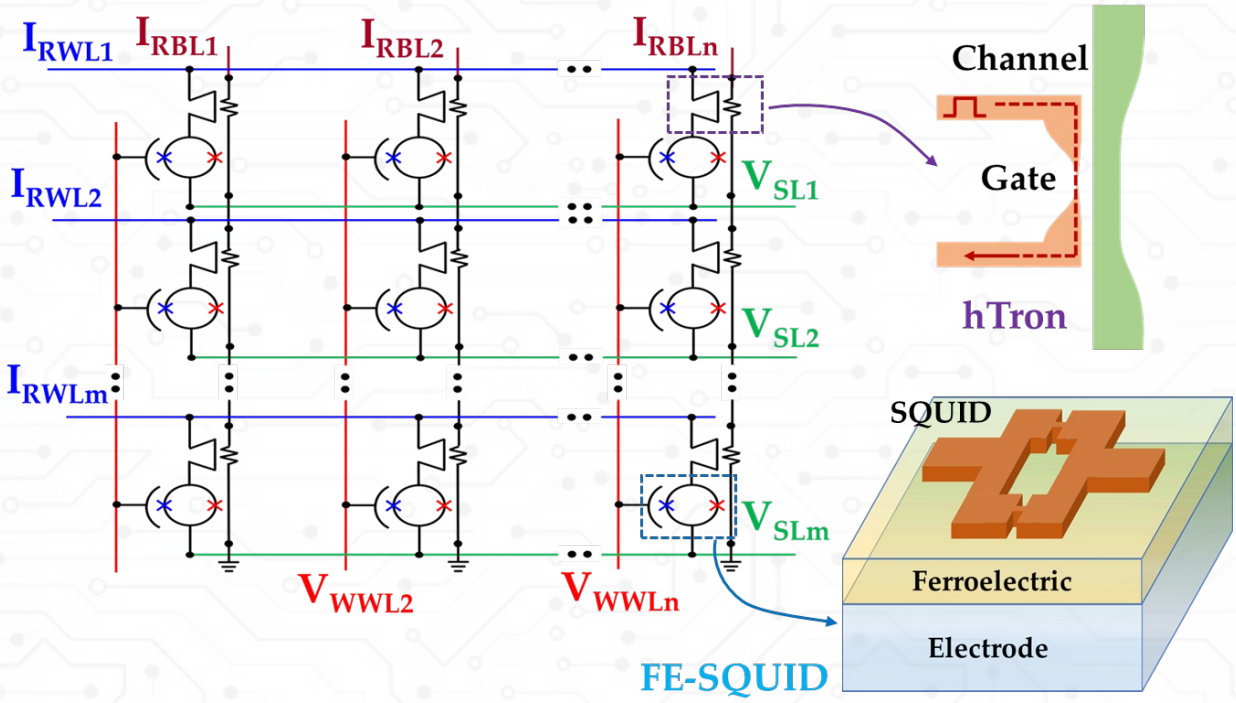
An illustration of the artificial synapse topology highlighting the superconducting memristor (SM) elements, as well as the heater cryotrons, which work to offer up to 8 different synaptic weights.

This technology is patent pending.

Superconducting Non-Volatile Memory

Cryogenic Memory Array based on Ferroelectric SQUID and Heater Cryotron

Dr. Ahmedullah Aziz has developed a non-volatile memory system utilizing a unique device called the ferroelectric superconducting quantum interference device (FE-SQUID) in order to tackle the lack of a scalable and compatible cryogenic memory system, which has been a major obstacle to the widespread adoption of several promising fields such as quantum computers, superconducting processors, and cryogenic neuromorphic systems. The developed memory system features several key advantages such as excellent scalability, simple sensing circuitry, voltage-based write operation, and separate read-write paths. An essential feature of this memory system is the use of the superconducting SQUID for the read operation. This not only enables efficient memory read operations but also opens up possibilities for cryogenic in-memory computing with ultra-low power consumption.



Non-volatile cryogenic memory system utilizing Ferroelectric SQUID as the memory element and heater cryotron as the access device. This unique memory system is specially suited to serve the needs of quantum computing, cryogenic neuromorphic system, and superconducting electronics

This technology is patent pending.